Triple Output Power Supply for Small TFT-LCD Displays

FEATURES

- **Generates Three Voltages:**
  5.1V at 10mA
  –5V, –10V, or –15V at 500µA
  10V or 15V at 500µA
- **Better than 90% Efficiency**
- **Low Output Ripple: Less than 5mV$_{P-P}$**
- **Complete 1mm Component Profile Solution**
- Controlled Power-Up Sequence: AV$_{DD}$/V$_{GL}$/V$_{GH}$
- All Outputs Disconnected and Actively Discharged in Shutdown
- Low Noise Fixed Frequency Operation
- Frequency Reduction Input for High Efficiency in Blank Mode
- Ultralow Quiescent Current: 75µA (Typ) in Scan Mode
- Available in a 3mm × 3mm 16-Pin QFN Package

APPLICATIONS

- Cellular Handsets with Color Display
- Handheld Instruments
- PDA

DESCRIPTION

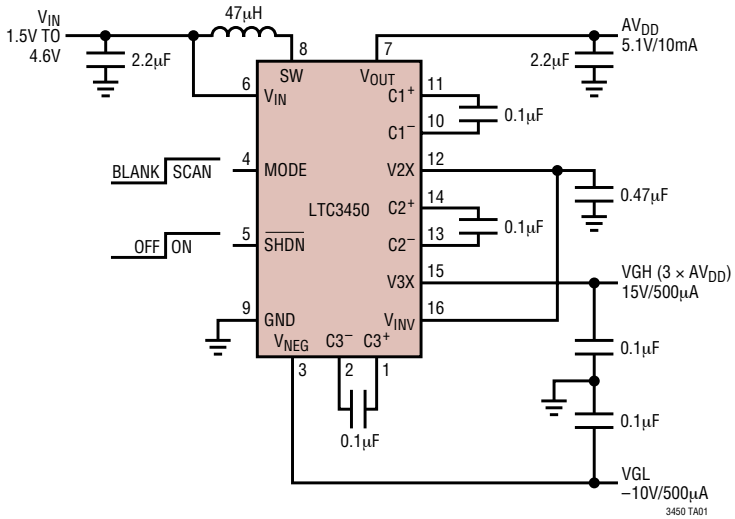
The LTC®3450 is a complete power converter solution for small thin film transistor (TFT) liquid crystal display (LCD) panels. The device operates from a single Lithium-Ion cell, 2- to 3-cell alkaline input or any voltage source between 1.5V and 4.6V.

The synchronous boost converter generates a low noise, high efficiency 5.1V, 10mA supply. Internal charge pumps are used to generate 10V, 15V, and –5V, –10V or –15V. Output sequencing is controlled internally to insure proper initialization of the LCD panel.

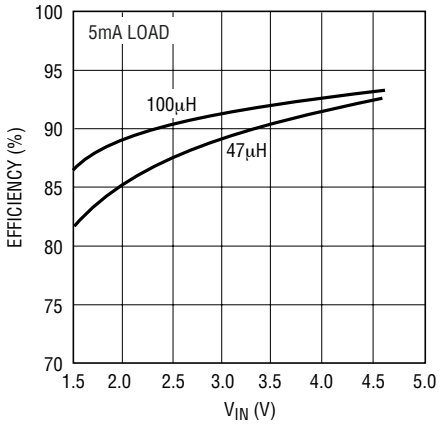
A master shutdown input reduces quiescent current to <2µA and quickly discharges each output for rapid turn off of the LCD panel. The LTC3450 is offered in a low profile (0.75mm), 3mm × 3mm 16-pin QFN package, minimizing the solution profile and footprint.

TYPICAL APPLICATION

5.1V, –10V, 15V Triple Output TFT-LCD Supply



AV$_{DD}$ Efficiency vs V$_{IN}$

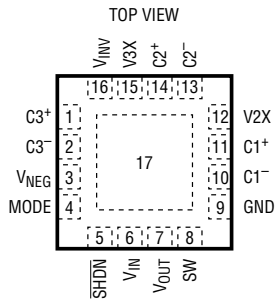


ABSOLUTE MAXIMUM RATINGS

(Note 1) (Referred to GND)

V_{IN}, SW ..... –0.3 to 7V
$\overline{SHDN}$, MODE ..... –0.3 to 7V
V_{OUT} ..... –0.3 to 5.5V
V_{NEG} ..... –17V to 0.3V
Operating Temperature Range
LTC3450E (Note 4) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
EXPOSED PAD IS V_{NEG} (PIN 17)
MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 68°C/W

ORDER PART NUMBER
LTC3450EUD
UD PART MARKING
LAAC

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{OUT} = 5.2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	1.5		4.6	V
V_{IN} Quiescent Supply Current	MODE = V_{IN}			75	130	µA
V_{OUT} Quiescent Supply Current	MODE = V_{IN}			80		µA
V_{IN} Quiescent Supply Current	MODE = GND			30	50	µA
V_{OUT} Quiescent Supply Current	MODE = GND			13		µA
V_{IN} Quiescent Current	$\overline{SHDN}$ = GND, V_{OUT} OPEN			0.01	2	µA
5V Boost Regulator						
V_{OUT} Output Voltage	Load on V_{OUT} = 5mA		5.049	5.100	5.151	V
V_{OUT} Efficiency	Load on V_{OUT} = 5mA, (Note 2)			90		%
V_{OUT} Maximum Output Current	L = 47µH, (Note 2)			11		mA
Switch Current Limit			90	120		mA
Switching Frequency—Boost	MODE = V_{IN}			550		kHz
Switching Frequency—Boost	MODE = GND			15.62		kHz
Charge Pumps						
V2X Output Voltage	Load on V2X = 100µA	●	9.792	10.1	10.608	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{OUT} = 5.2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V3X Output Voltage	Load on V3X = 100µA	●	14.688	15.2	15.912	V
V2X Efficiency	Load on V2X = 100µA, (Note 2)			90		%
V3X Efficiency	Load on V3X = 100µA, (Note 2)			80		%
Output Impedance V2X, V3X	Flying Capacitors = 0.1µF			1		kΩ
V_{NEG} Output Voltage	Load on V_{NEG} = 100µA, V_{INV} = V2X	●	–10.608	–10.1	–9.792	V
V_{NEG} Efficiency	Load on V_{NEG} = 100µA (Note 2)			80		%
Output Impedance V_{NEG}	Flying Capacitor = 0.1µF			1		kΩ
Switching Frequency Charge Pumps	MODE = V_{IN}			62.5		kHz
Switching Frequency Charge Pumps	MODE = GND			3.75		kHz
V_{NEG} to V3X Delay	(Note 3)		3	4	10	ms
Logic Inputs						
$\overline{SHDN}$ Pin Threshold		●	0.4	0.77	1.2	V
MODE Pin Threshold				1.6		V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

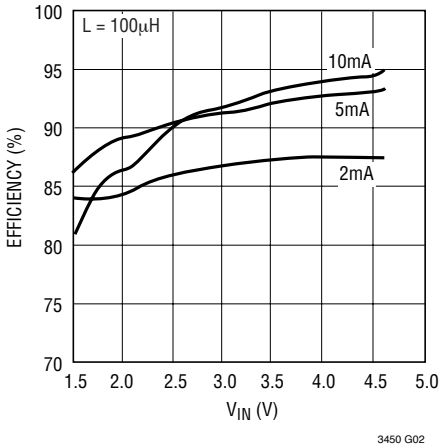
Note 2: Specification is guaranteed by design and not 100% tested in production.

Note 3: Measured from point at which V_{NEG} crosses –5V to point at which $C2^-$ starts switching.

Note 4: The LTC3450E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

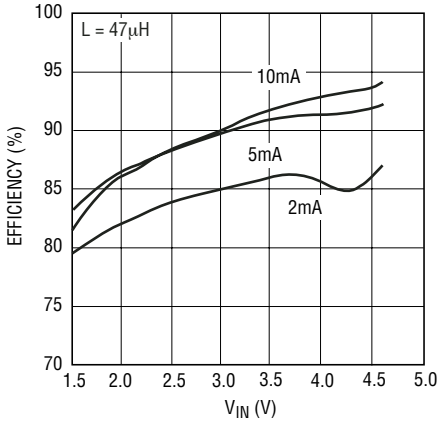
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

AV_{DD} Efficiency vs V_{IN}



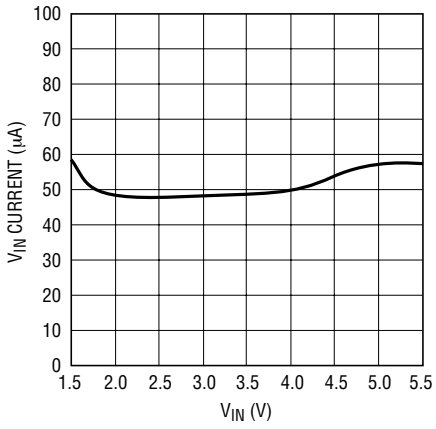
3450 G02

AV_{DD} Efficiency vs V_{IN}



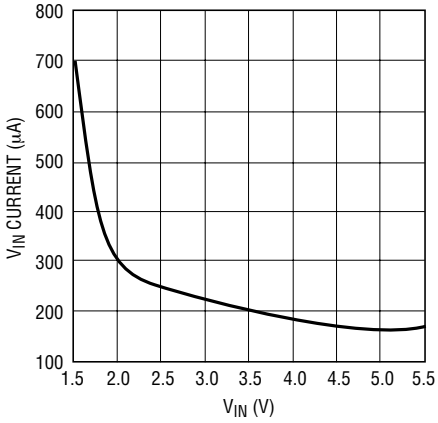
3450 G03

No Load V_{IN} Current in Blank Mode



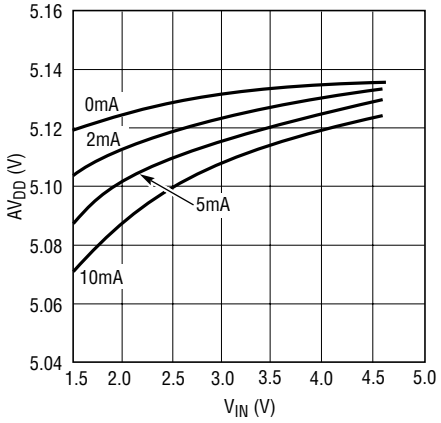
3450 G04

No Load V_{IN} Current in Scan Mode



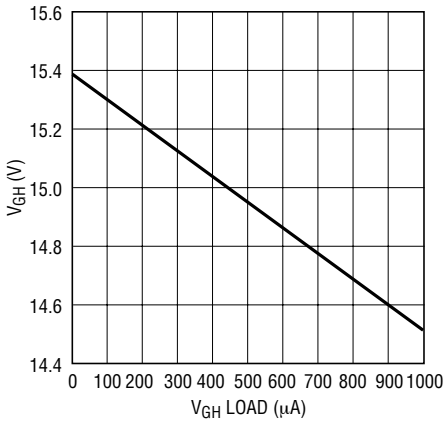
3450 G05

AV_{DD} vs V_{IN} and Load



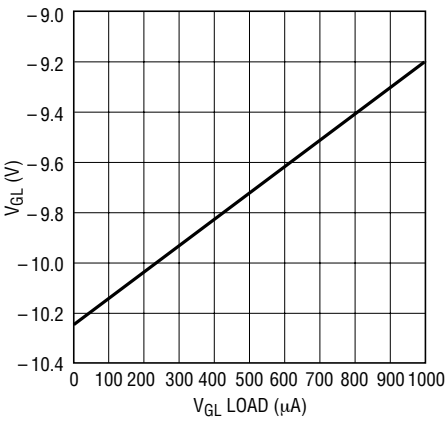
3450 G06

V_{GH} vs Load



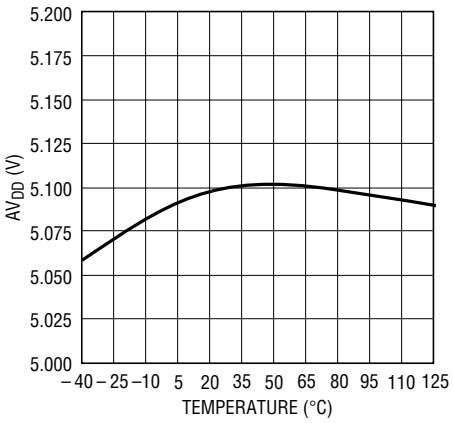
3450 G07

V_{GL} vs Load



3450 G08

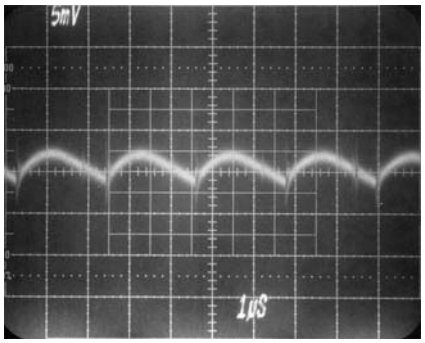
AV_{DD} vs Temperature
Figure 1 Circuit, 1mA Load



3450 G09

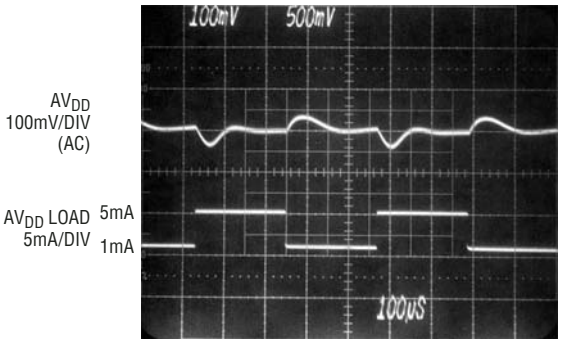
TYPICAL PERFORMANCE CHARACTERISTICS

AV_{DD} Ripple Voltage
AV_{DD} Load = 5mA



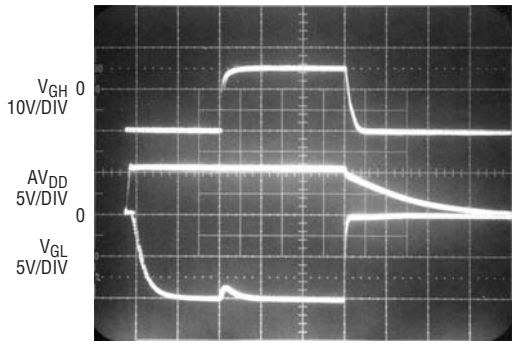
V_{IN} = 3.6V
C2 = 2.2µF
1µs/DIV
3450 G10

AV_{DD} Transient Response



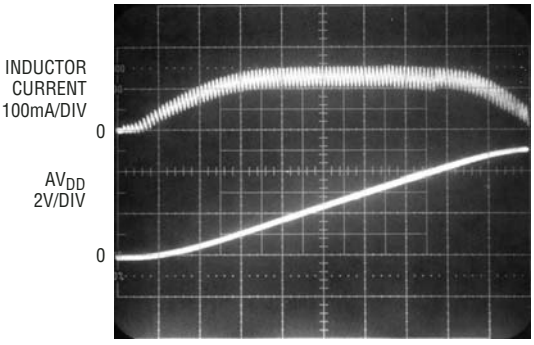
V_{IN} = 3.6V
C2 = 2.2µF
100µs/DIV
3450 G11

AV_{DD}, V_{GL}, V_{GH} Turn-On and Turn-Off Sequence



V_{IN} = 3.6V
C2 = 2.2µF
2ms/DIV
3450 G12

AV_{DD} Turn-On Showing Inrush Current Limiting



V_{IN} = 3.6V
20µs/DIV
3450 G13

PIN FUNCTIONS

$C3^+$ (Pin 1): Charge Pump Inverter Flying Capacitor Positive Node. The charge pump inverter flying capacitor is connected between $C3^+$ and $C3^-$. The voltage on $C3^+$ will alternate between GND and V_{INV} at an approximate 50% duty cycle while the inverting charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

$C3^-$ (Pin 2): Charge Pump Inverter Flying Capacitor Negative Node. The charge pump inverter flying capacitor is connected between $C3^+$ and $C3^-$. The voltage on $C3^-$ will alternate between GND and V_{NEG} at an approximate 50% duty cycle while the inverting charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

V_{NEG} (Pin 3): Charge Pump Inverter Output. V_{NEG} can be either –5V or –10V depending on where V_{INV} is connected. V_{NEG} should be bypassed to GND with at 0.1µF or larger X5R type ceramic capacitor. V_{NEG} can also be configured for –15V with two external low current Schottky diodes (see Applications section).

MODE (Pin 4): Drive MODE high to force the LTC3450 into high power (scan) mode. Drive MODE low to force the LTC3450 into low power (blank) mode. The output voltages remain active with the MODE pin driven low but with reduced output current capability. MODE must be pulled up to V_{IN} or higher on initial application of power in order for proper initialization to occur.

$\overline{SHDN}$ (Pin 5): Master Shutdown Input for the LTC3450. Driving $\overline{SHDN}$ low disables all IC functions and reduces quiescent current from the battery to less than 2µA. Each generated output voltage is actively discharged to GND in shutdown through internal pull down devices. An optional RC network on $\overline{SHDN}$ provides a slower ramp up of the boost converter inductor current during startup (soft-start).

V_{IN} (Pin 6): Input Supply to the LTC3450. Connect V_{IN} to a voltage source between 1.5V and 4.6V. Bypass V_{IN} to GND with a 2.2µF X5R ceramic capacitor.

V_{OUT} (Pin 7): Main 5.1V Output of the Boost Regulator and Input to the Voltage Doubler Stage. Bypass V_{OUT} with a low ESR, ESL ceramic capacitor (X5R type) between 2.2µF and 10µF.

SW (Pin 8): Switch Pin. Connect the inductor between SW and V_{IN}. Keep PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero, the internal P-channel MOSFET synchronous rectifier is turned off to prevent reverse charging of the inductor and an internal switch connects SW to V_{IN} to reduce EMI.

GND (Pin 9): Signal and Power Ground for the LTC3450. Provide a short direct PCB path between GND and the output filter capacitor(s) on V_{OUT}, V2X, V3X and V_{NEG}.

$C1^-$ (Pin 10): Charge Pump Doubler Flying Capacitor Negative Node. The charge pump doubler flying capacitor is connected between $C1^+$ and $C1^-$. The voltage on $C1^-$ will alternate between GND and V_{OUT} at an approximate 50% duty cycle while the charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

$C1^+$ (Pin 11): Charge Pump Doubler Flying Capacitor Positive Node. The charge pump doubler flying capacitor is connected between $C1^+$ and $C1^-$. The voltage on $C1^+$ will alternate between V_{OUT} and V2X at an approximate 50% duty cycle while the charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

V2X (Pin 12): Charge Pump Doubler Output. This output is 10.2V (nom) at no load and is capable of delivering up to 500µA to a load. V2X should be bypassed to GND with a 0.47µF X5R type ceramic capacitor.

$C2^-$ (Pin 13): Charge Pump Tripler Flying Capacitor Negative Node. The charge pump tripler flying capacitor is connected between $C2^+$ and $C2^-$. The voltage on $C2^-$ will alternate between GND and V_{OUT} at an approximate 50% duty cycle while the charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

$C2^+$ (Pin 14): Charge Pump Tripler Flying Capacitor Positive Node. The charge pump tripler flying capacitor is connected between $C2^+$ and $C2^-$. The voltage on $C2^+$ will alternate between V2X and V3X at an approximate 50% duty cycle while the charge pump is operating. Use a 10nF or larger X5R type ceramic capacitor for best results.

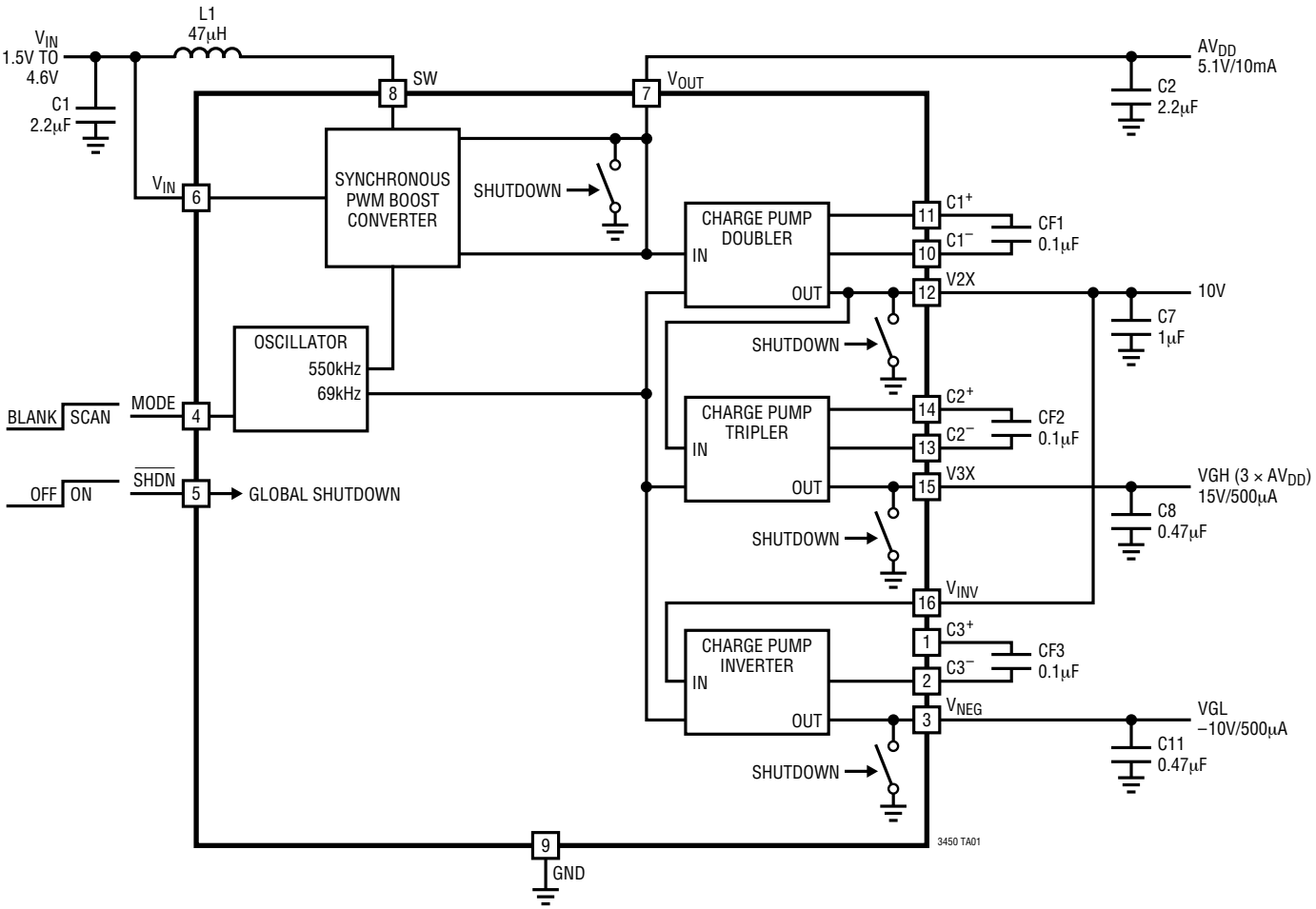
PIN FUNCTIONS

V3X (Pin 15): Charge Pump Tripler Output. This output is 15.3V (nom) at no load and is capable of delivering up to 500μA to a load. V3X should be bypassed to GND with a 0.1μF X5R type ceramic capacitor.

V_{INV} (Pin 16): Positive Voltage Input for the Charge Pump Inverter. The charge pump inverter will generate a negative voltage corresponding to the voltage applied to V_{INV}. Connecting V_{INV} to 5V or 10V will generate –5V or –10V respectively on V_{NEG}. See Applications section for –15V generation.

Exposed Pad (Pin 17): The exposed pad must be connected to V_{NEG} (Pin 3) on the PCB. ***Do not connect the exposed pad to GND.***

BLOCK DIAGRAM



OPERATION

The LTC3450 is a highly integrated power converter intended for small TFT-LCD display modules. A fixed frequency, synchronous PWM boost regulator generates a low noise 5.1V, 10mA bias at greater than 90% efficiency from an input voltage of 1.5V to 4.6V. Three charge pump converters use the 5.1V output to generate 10V, 15V and –5V, –10V or –15V at load currents up to 500μA. Each converter is frequency synchronized to the main 550kHz (nominal) boost converter. The generated output voltages are internally sequenced to insure proper initialization of the LCD panel. A digital shutdown input rapidly discharges each generated output voltage to provide a near instantaneous turn-off of the LCD display.

Boost Converter

The synchronous boost converter utilizes current mode control and includes internally set control loop and slope compensation for optimized performance and simple design. Only three external components are required to complete the design of the 5.1V, 10mA boost converter. The high operation frequency produces very low output ripple and allows the use of small low profile inductors and tiny external ceramic capacitors. The boost converter also disconnects its output from V_{IN} during shutdown to avoid loading the input power source. Softstart produces a controlled ramp of the converter input current during startup, reducing the burden on the input power source. Very low operating quiescent current and synchronous operation allow for greater than 90% conversion efficiency.

The MODE input reduces the boost converter operating frequency by approximately 8x when driven high and reduces the output power capability of the boost converter. MODE is asserted when the polysilicon TFT-LCD display is in its extremely low power blank condition. The boost converter further reduces its quiescent current in this mode, delivering both lower input (battery) current drain and low noise operation.

Charge Pumps

The LTC3450 includes three separate charge pump converters which generate 10V, 15V and either –5V, –10V or –15V. Each output can deliver a maximum of 500μA. The charge pumps feature fixed frequency, open-loop operation for high efficiency and lowest noise performance. The charge pump converters operate at 1/8 the boost converter frequency and include internal charge transfer switches. Thus, each charge pump requires only two small external capacitors, one to transfer charge, and one for filtering. Similar to the boost converter, the charge pumps operating frequency reduces to approximately 4kHz in blank mode, maintaining low noise operation but at reduced output current capability.

Output Sequencing

Refer to the following text and Figure 1 for the LTC3450 power-up sequence. When input power is applied, the boost converter initializes and charges its output towards the final value of 5.1V. When the boost converter output reaches approximately 90% of its final value (4.5V), an internal 5V OK signal is asserted which allows the charge pump doubler to begin operation toward its final goal of 10V. Approximately 1ms later, the charge pump inverter begins operation toward its final goal of either –5V or –10V depending on the connection of the V_{INV} input. When the –5V or –10V output (V_{NEG}) reaches approximately 50% of its final value, a 4ms (nominal) timeout period begins. At the conclusion of the 4ms timeout period, the charge pump tripler is allowed to begin operation, which will eventually charge V3X to 15V (nominal).

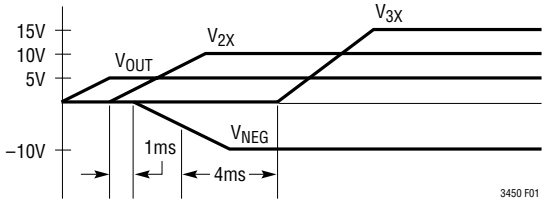


Figure 1. Output Sequencing

APPLICATIONS INFORMATION

Inductor Selection

Inductors in the range of 47μH to 100μH with saturation current (I_{SAT}) ratings of at least 150mA are recommended for use with the LTC3450. Ferrite core materials are strongly recommended for their superior high frequency performance characteristics. A bobbin or toroid type core will reduce radiated noise. Inductors meeting these requirements are listed in Table 1.

Table 1. Recommended Inductors

PART NUMBER	L (μH)	MAX DCR (Ω)	HEIGHT (mm)	VENDOR
CLQ4D10-470	47	1.28	1.2	Sumida
CLQ4D10-101	100	3.15		(847) 956-0666
CMD4D08-470	47	1.6	1.0	www.sumida.com
DO1606-473	47	1.1	2.0	Coilcraft
DO1606-104	100	2.3		(847) 639-6400
DT1608-473	47	0.34	2.92	www.coilcraft.com
DT1608-104	100	1.1		
LQH43MN470J03	47	1.5	2.6	Murata
LQH43MN101J03	100	2.5		www.murata.com
DU6629-470M	47	0.64	2.92	Coev Magnetics
DU6629-101M	100	1.27		www.circuitprotection.com

Capacitor Selection

The boost converter requires two capacitors. The input capacitor should be an X5R type of at least 1μF. The V_{OUT} capacitor should also be an X5R type between 2.2μF and 10μF. A larger capacitor (10μF) should be used if lower output ripple is desired or the output load required is close to the 10mA maximum.

The charge pumps require flying capacitors of at least 0.1μF to obtain specified performance. Ceramic X5R types are strongly recommended for their low ESR and ESL and capacitance versus bias voltage stability. The filter capacitor on V2X should be at least 0.1μF. A 0.47μF or larger capacitor on V2X is recommended if V_{INV} is connected to V2X. The filter capacitors on V3X and V_{NEG} should be 0.1μF or larger. Please be certain that the capacitors used are rated for the maximum voltage with adequate safety margin. Refer to Table 2 for a listing of capacitor vendors.

Table 2. Capacitor Vendor Information

Supplier	Phone	Website
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com
Taiyo Yuden	(408) 573-4150	www.t-yuden.com

Soft-Start

Soft-start operation provides a gradual increase in the current drawn from the input power source (usually a battery) during initial startup of the LTC3450, eliminating the inrush current which is typical in most boost converters. This reduces stress on the input power source, boost inductor and output capacitor, reduces voltage sag on the battery and increases battery life. The rate at which the input current will increase is set by two external components (R_{SS} and C_{SS}) connected to $\overline{SHDN}$ (refer to Figure 2). Upon initial application of power or release of a pull down switch on $\overline{SHDN}$, the voltage on $\overline{SHDN}$ will increase relative to the R • C time constant or R_{SS} • C_{SS}. After one time constant $\overline{SHDN}$ will rise to approximately 63.2% of the voltage on V_{IN}. From 0V to approximately 0.77V on $\overline{SHDN}$, no switching will occur because the shutdown threshold is 0.77V (typ). From 0.77V to 1V the maximum switch pin current capability of the LTC3450 will gradually increase from near zero to the maximum current limit. An R_{SS} in the range of 1MΩ to 10MΩ is recommended. If $\overline{SHDN}$ is driven high with a logic signal, the input current will gradually increase to its maximum value in approximately 50μs.

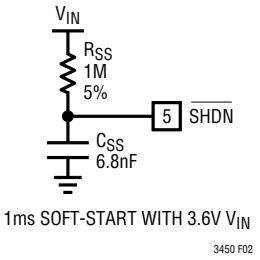
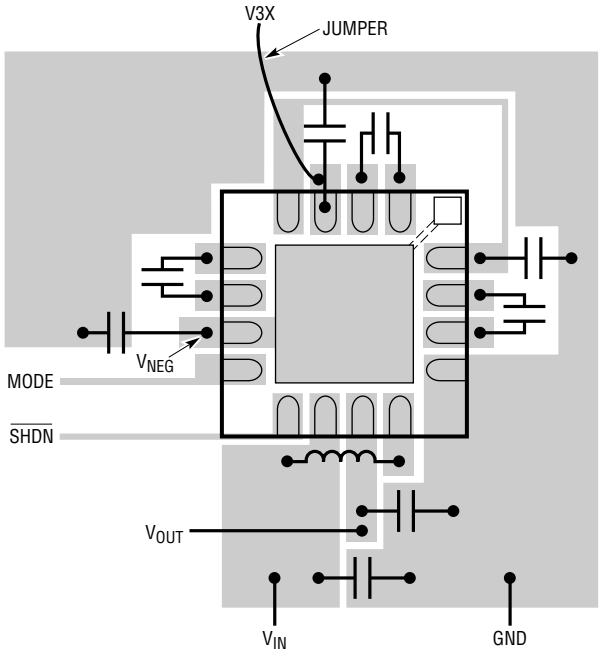


Figure 2. Soft-Start Component Configuration

Printed Circuit Board Layout Guidelines

High speed operation of the LTC3450 demands careful attention to PCB layout. You will not get advertised performance with careless layout. Figure 3 shows the recommended component placement for a single layer PCB. A multilayer board with a separate ground plane is ideal but not absolutely necessary.

APPLICATIONS INFORMATION



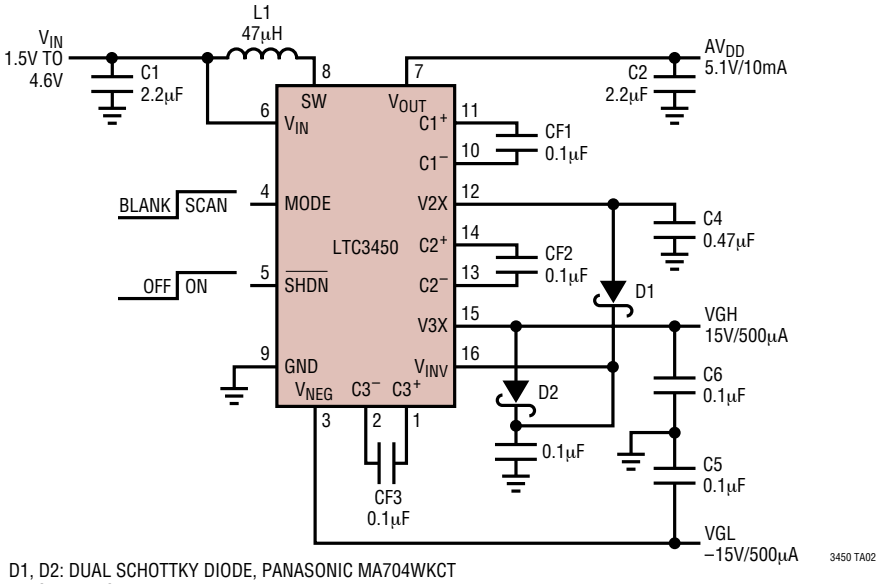
NOTE: QFN PACKAGE EXPOSED PAD
IS CONNECTED TO THE V_{NEG} PIN.
DO NOT CONNECT EXPOSED PAD TO GROUND

3450 F03

Figure 3. Suggested Layout

TYPICAL APPLICATION

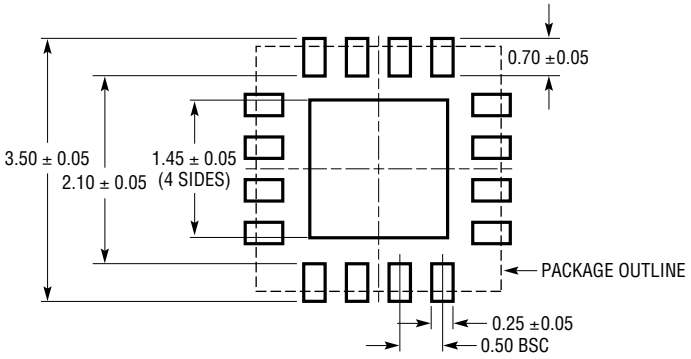
5.1V, –15V, 15V Triple Output TFT-LCD Supply



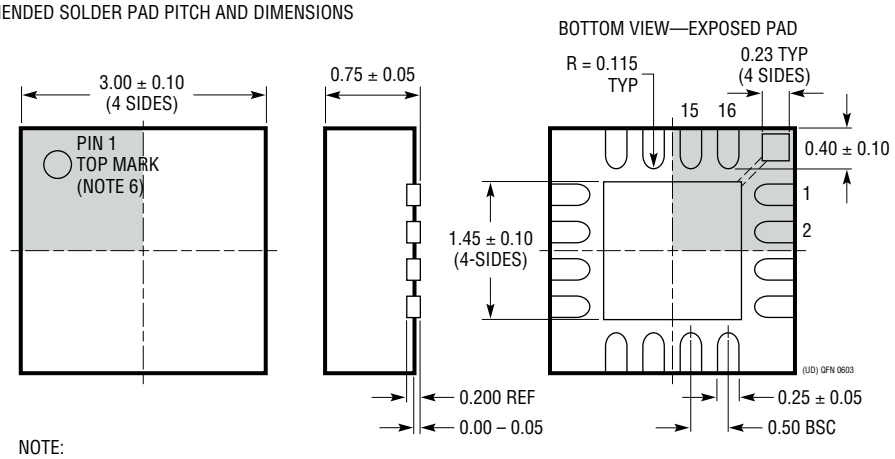
D1, D2: DUAL SCHOTTKY DIODE, PANASONIC MA704WKCT
L1: SUMIDA CMD4D08-470

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



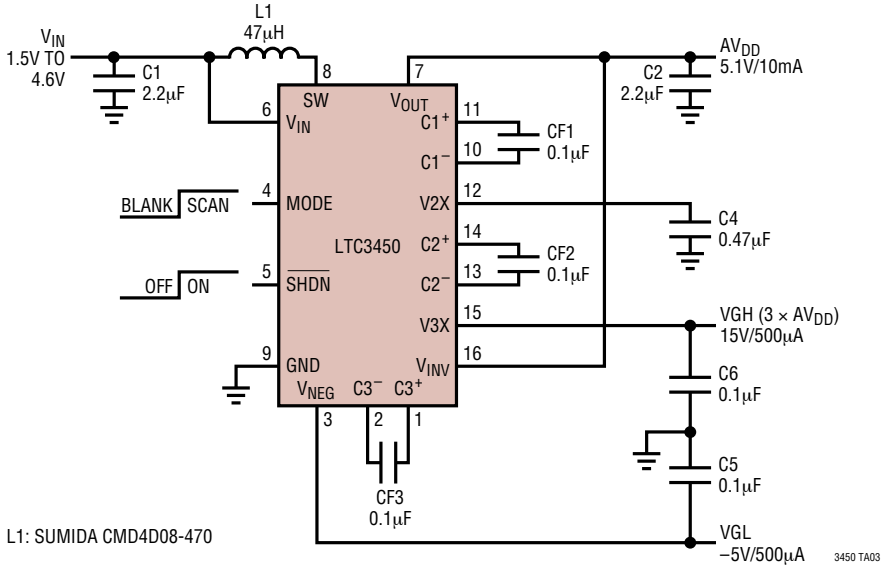
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

5.1V, –5V, 15V Triple Output TFT-LCD Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1310	1.5A I_{SW}, 4.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.75V to 18V, V_{OUT} = 35V, I_Q = 12mA, I_{SD} = <1µA MSE Package
LT1613	550mA I_{SW}, 1.4MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 0.9V to 10V, V_{OUT} = 34V, I_Q = 3mA, I_{SD} = <1µA ThinSOT Package
LT1615/LT1615-1	300mA/80mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, V_{OUT} = 34V, I_Q = 20µA, I_{SD} = <1µA ThinSOT Package
LT1940	Dual Output 1.4A I_{OUT}, Constant 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, V_{OUT} (MIN) = 1.2V, I_Q = 2.5mA, I_{SD} = <1µA TSSOP-16E Package
LT1944	Dual Output 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, V_{OUT} = 34V, I_Q = 20µA, I_{SD} = <1µA MS Package
LT1944-1	Dual Output 150mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, V_{OUT} = 34V, I_Q = 20µA, I_{SD} = <1µA MS Package
LT1945	Dual Output, Pos/Neg, 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, V_{OUT} = ±34V, I_Q = 20µA, I_{SD} = <1µA MS Package
LT1946/LT1946A	1.5A I_{SW}, 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.45V to 16V, V_{OUT} = 34V, I_Q = 3.2mA, I_{SD} = <1µA MS8 Package
LT1947	Triple Output (for TFT-LCD) 1.1A I_{SW}, 3MHz High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.7V to 8V, V_{OUT} = 34V, I_Q = 9.5mA, I_{SD} = <1µA MS Package
LT1949/LT1949-1	550mA I_{SW}, 600kHz/1.1MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.5V to 12V, V_{OUT} = 28V, I_Q = 4.5mA, I_{SD} = <25µA S8, MS8 Packages
LTC3400/LTC3400B	600mA I_{SW}, 1.2MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.85V to 5V, V_{OUT} = 5V, I_Q = 19µA/300µA, I_{SD} = <1µA ThinSOT Package
LTC3401	1A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, V_{OUT} = 5V, I_Q = 38µA, I_{SD} = <1µA, MS Package
LTC3402	2A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, V_{OUT} = 5V, I_Q = 38µA, I_{SD} = <1µA, MS Package

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